**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1 (currently amended): A method of manufacturing a semiconductor device having a tunnel oxide layer ~~for monitoring a tunnel oxide layer~~, the method comprising:

(a) providing a semiconductor substrate and forming at least one memory cell on a surface of the semiconductor substrate, the memory cell comprising a first gate, a second gate, and the tunnel oxide layer from top to bottom in a stack;

(b) electrically connecting the first gate and the second gate;

(c) applying a first gate voltage to the first gate, the first gate voltage being a swing time-dependent DC ramping voltage;

(d) measuring a first gate leakage current of the memory cell to calculate a first constant from an equation;

(e) applying a second gate voltage to the first gate, the second gate voltage being a swing time-dependent DC ramping voltage;

(f) measuring a second gate leakage current of the memory cell to calculate a second constant from the equation;

(g) calculating a first ratio of the second constant to the first constant; and

(h) performing a comparing step to compare the value of the first ratio with a predetermined value.

Claim 2 (previously presented): The method of claim 1 wherein the semiconductor substrate is a silicon substrate of a semiconductor wafer and the memory cell is formed in a testing area of the semiconductor wafer.

Claim 3 (original): The method of claim 1 wherein the memory cell is a flash memory cell, the first gate and the second gate are a controlling gate and a floating gate of the flash memory cell respectively.

Claim 4 (original): The method of claim 1 wherein the memory cell is a non-volatile memory cell, the first gate and the second gate are a controlling gate and a floating gate of the non-volatile memory cell respectively.

Claim 5 (original): The method of claim 1 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

Claim 6 (previously presented): The method of claim 1 wherein the equation is the Fowler-Nordheim tunneling mechanism equation.

Claim 7 (original): The method of claim 1 wherein the predetermined value is 10.

Claim 8 (original): The method of claim 1 wherein each constant is a . value corresponding to each gate voltage respectively.

Claim 9 (previously presented): The method of claim 8 wherein the first constant is a . 1 value corresponding to the first gate voltage and the . 1 value is equal to 【{△ln[|the first gate leakage current|/ (|the first gate voltage|-|a flatband voltage($V_{fb}$)|) $^2$]}÷{△[1 ÷(|the first gate voltage|-|the flatband voltage|)]}】.

Claim 10 (currently amended): The method of claim 8 wherein the second constant is a . 2 value corresponding to the second gate voltage

and the . 2 value is equal to 【{△ln[|the second gate leakage current|/(|the second gate voltage|-|[[the]] a flatband voltage($V_{fb}$)|)$^2$]}÷{△[1÷(|the second gate voltage|-|the flatband voltage|)]}】.

Claim 11 (currently amended): The method of claim 8 further comprising the following steps when the value of the first ratio is not greater than the predetermined value:

applying a third gate voltage to the first gate, the third gate voltage [[is]] being a swing time-dependent DC ramping voltage;

measuring a third gate leakage current of the memory cell to calculate a third constant from the equation;

calculating a second ratio of the third constant to the second constant; and

performing the comparing step to compare the value of the second ratio with the predetermined value.

Claim 12 (original): The method of claim 11 wherein the steps (c) to (h) are repeated when the value of the second ratio is not greater than the predetermined value.

Claim 13 (original): The method of claim 11 wherein the quality of the tunnel oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

Claim 14 (previously presented): The method of claim 11 wherein the third constant is a . 3 value corresponding to the third gate voltage and the . 3 value is equal to 【{△ln[|the third gate leakage current|/(|the third gate voltage|-|a flatband voltage($V_{fb}$)|)$^2$]}÷{△[1÷(|the third gate voltage|-|the flatband voltage|)]}】.

Claim 15 (currently amended): The method of claim 14 further

comprising ~~a step for~~ plotting a . -$V_g$ curve of each . value respectively corresponding to the first gate voltage, the second gate voltage and the third gate voltage versus the first gate voltage, the second gate voltage and the third gate voltage, and comparing a reference . -$V_g$ curve for the unstress-induced tunnel oxide layer in the memory cell ~~is compared~~ with the . -$V_g$ curve to monitor the quality of the tunnel oxide layer.

Claim 16 (original): The method of claim 15 wherein the . -$V_g$ curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

Claim 17 (currently amended): The method of claim 16 wherein the . value within the first region is zero to represent each gate leakage current flowing through the first gate and the second gate in the memory cell being less than a predetermined current value, the absolute value of the . value within the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each gate leakage current of the memory cell, and the . value within the third region crosses the reference . -$V_g$ curve to represent a plurality of carriers being trapped by the tunnel oxide layer.

Claim 18 (original): The method of claim 17 wherein the predetermined current value is $1.0x10^{-11}$A.

Claim 19 (currently amended): The method of claim 8 further comprising ~~a step for~~ plotting a . -$V_g$ curve of each . value versus each gate voltage, and comparing a reference . -$V_g$ curve for the unstress-induced tunnel oxide layer in the memory cell ~~is compared~~ with the . -$V_g$ curve to monitor the quality of the tunnel oxide layer.

Claim 20 (original): The method of claim 1 wherein the method is applied to a wafer acceptance testing (WAT) equipment to fast monitor

the stress-induced degradation of the tunnel oxide layer in the memory cell.

Claim 21 (currently amended) A method of manufacturing a semiconductor device having an oxide layer ~~for fast monitoring the stress induced degradation of an oxide layer by a wafer acceptance testing (WAT) equipment~~, the method comprising:

(a) providing a substrate, a surface of the substrate comprising the oxide layer and a first conductive layer disposed on the oxide layer;

(b) applying a first voltage to the first conductive layer, the first voltage being a swing time-dependent DC ramping voltage;

(c) measuring a first leakage current flowing through the first conductive layer to calculate a first proportional value from the first voltage, the first leakage current, and an equation, the first proportional value corresponding to the first voltage;

(d) applying a second voltage to the first conductive layer, the second voltage being a swing time-dependent DC ramping voltage;

(e) measuring a second leakage current flowing through the first conductive layer to calculate a second proportional value from the second voltage, the second leakage current, and the equation, the second proportional value corresponding to the second voltage; and

(f) calculating a first ratio of the second proportional value to the first proportional value.

Claim 22 (previously presented): The method of claim 21 wherein the substrate is a silicon substrate of a semiconductor wafer and the first conductive layer is formed in a testing area of the semiconductor wafer.

Claim 23 (previously presented): The method of claim 21 wherein a second conductive layer is formed between the first conductive layer and the oxide layer.

Claim 24 (previously presented): The method of claim 23 further comprising an electrically connecting step performed before applying the first voltage to the first conductive layer to electrically connect the first conductive layer and the second conductive layer.

Claim 25 (previously presented): The method of claim 24 wherein the first conductive layer and the second conductive layer are a controlling gate and a floating gate of a flash memory cell respectively, and the oxide layer is a tunnel oxide layer of the flash memory cell.

Claim 26 (currently amended): The method of claim 24 wherein the first conductive layer is a controlling gate of a non-volatile memory cell, the second conductive layer is a floating gate of the non-volatile memory cell, and the oxide layer is a tunnel oxide layer of the non-volatile memory cell.

Claim 27 (previously presented): The method of claim 21 wherein the first conductive layer is a gate of a metal-oxide-semiconductor (MOS) transistor, the oxide layer is a gate oxide layer of the MOS transistor.

Claim 28 (previously presented): The method of claim 21 further comprising a comparing step to compare the value of the first ratio with a predetermined value.

Claim 29 (previously presented): The method of claim 28 wherein the quality of the oxide layer is degenerated to be not acceptable when the value of the first ratio is greater than the predetermined value.

Claim 30 (original): The method of claim 28 wherein the predetermined value is 10.

Claim 31 (previously presented): The method of claim 21 wherein the

equation is the Fowler-Nordheim tunneling mechanism equation.

Claim 32 (previously presented): The method of claim 28 wherein each proportional value is a . value corresponding to each voltage respectively.

Claim 33 (previously presented): The method of claim 32 wherein the first proportional value is a . 1 value corresponding to the first voltage and the . 1 value is equal to 【{△ln[|the first leakage current|/(|the first voltage|-|a flatband voltage($V_{fb}$)|)$^2$]}÷{△[1 ÷(|the first voltage|-|the flatband voltage|)]}】.

Claim 34 (currently amended): The method of claim 32 wherein the second proportional value is a . 2 value corresponding to the second voltage and the . 2 value is equal to 【{△ln[|the second leakage current|/(|the second voltage|-|[[the]] a flatband voltage($V_{fb}$)|)$^2$]}÷{△[1÷(|the second voltage|-|the flatband voltage|)]}】.

Claim 35 (currently amended): The method of claim 32 further comprising the following steps when the value of the first ratio is not greater than the predetermined value:

applying a third voltage to the first conductive layer, the third voltage [[is]] being a swing time-dependent DC ramping voltage;

measuring a third leakage current flowing through the first conductive layer;

calculating a third proportional value from the third voltage, the third leakage current, and the equation, the third proportional value corresponding to the third voltage;

calculating a second ratio of the third proportional value to the second proportional value; and

performing the comparing step to compare the value of the second

ratio with the predetermined value.

Claim 36 (original): The method of claim 35 wherein the steps (b) to (f) are repeated when the value of the second ratio is not greater than the predetermined value.

Claim 37 (original): The method of claim 35 wherein the quality of the oxide layer is degenerated to be not acceptable when the value of the second ratio is greater than the predetermined value.

Claim 38 (previously presented): The method of claim 35 wherein the third proportional value is a . 3 value corresponding to the third voltage and the . 3 value is equal to 【{△ln[|the third leakage current|/ ( |the third voltage|-|a flatband voltage($V_{fb}$)| ) $^2$]} ÷ { △ [1 ÷ (|the third voltage|-|the flatband voltage|)]}】 .

Claim 39 (currently amended): The method of claim 38 further comprising ~~a step for~~ plotting a . -V curve of each . value respectively corresponding to the first voltage, the second voltage and the third voltage versus the first voltage, the second voltage and the third voltage, and comparing a reference . -V curve for the unstress-induced oxide layer ~~is compared~~ with the . -V curve to monitor the quality of the oxide layer.

Claim 40 (previously presented): The method of claim 39 wherein the . -V curve comprises at least a first region (region I), a second region (region II), and a third region (region III).

Claim 41 (currently amended): The method of claim 40 wherein the . value within the first region is zero to represent each leakage current flowing through the first conductive layer being less than a predetermined current value, the absolute value of the . value within

the second region increases to represent the stress-induced leakage current (SILC) resulting in the increase of each leakage current flowing through the first conductive layer, and the . value within the third region crosses the reference . -V curve to represent a plurality of carriers being trapped by the oxide layer.

Claim 42 (original): The method of claim 41 wherein the predetermined current value is $1.0x10^{-11}$A.

Claim 43 (currently amended): The method of claim 32 further comprising ~~a step for~~ plotting a . -V curve of each . value versus each voltage, and comparing a reference . -V curve for the unstress-induced oxide layer ~~is compared~~ with the . -V curve to monitor the quality of the oxide layer.